REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed December 11, 2003. Upon entry of the amendments identified above, claims 15 – 28 are pending in the application. Specifically, Applicants canceled claims 1 – 14 without prejudice, waiver, or disclaimer. Applicants amended claims 15 – 20 and added new claims 24 – 28. These amendments do not add any new matter to the application. Reconsideration and allowance of the application and all pending claims are respectfully requested.

I. Claims 15 – 28 are Patentable Over Cited Art

The Office Action rejects claims 1 – 12 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,924,111 to Huang *et al.* ("the '111 patent") in view of U.S. Patent No. 5,038,297 to Hannah ("the '297 patent"). The Office Action rejects claims 13 – 17 and 19 – 21 under 35 U.S.C. §103(a) as allegedly being unpatentable over Huang *et al.* in view of U.S. Patent No. 6,067,382 to Maeda ("the '382 patent"). The Office Action rejects claims 18 and 22 – 23 under 35 U.S.C. §103(a) as allegedly being unpatentable over the '111 patent in view the '297 patent and the '382 patent and further in view of U.S. Patent No. 5,544,306 to Deering ("the '306 patent").

Applicants respectfully submit that the rejection of claims 1 – 14 is rendered moot because Applicants canceled these claims. Claims 1 – 14 were canceled without prejudice, waiver, or disclaimer and merely to reduce the number of disputed issues.

With regard to rejected claims 15 – 23 and new claims 24 – 28, Applicants respectfully submit that each of these claims are patentable over the cited art because the cited art fails to disclose, teach, or suggest ALL of the features/limitations/elements contained in the claims.

In this regard, Applicants note that independent claims 15, 20, 21 and 24 each contain the features/limitations/elements of subdividing a memory region into a plurality of sub-regions and concurrently writing clear data to each of the plurality of sub-regions. Specifically, independent claim 15 is directed to a method for writing clear data to a frame buffer of a graphics display device. The method of claim 15 recites "subdividing said memory region into a plurality of sub-regions" and "writing said clear data concurrently to each of said plurality of sub-regions." Independent claim 20 is directed to a computer-readable medium having a program for clearing data residing in a region of a frame buffer" The program recites logic configured to "subdivide said memory region into a plurality of sub-regions" and "write said clear data concurrently to each of said plurality of sub-regions." Independent claims 21 is directed to a system which recites "means for subdividing said memory region into a plurality of sub-regions" and "means for writing said clear data concurrently to each of said plurality of sub-regions." Furthermore, new independent claim 24 is directed to a graphics system which recites logic configured to "subdivide the region of the frame buffer into a plurality of sub-regions" and "concurrently write clear data to each of the plurality of sub-regions."

Applicants respectfully submit that none of the cited references discloses, teaches, or otherwise suggests these claimed features. With regard to the '111 patent, Applicants respectfully disagree with the allegation in the Office Action that the reference discloses "subdividing a memory region into a plurality of sub-regions." First, Applicants submit that the '111 patent does not even disclose subdividing a region of memory into a plurality of sub-regions for the purpose of clearing data. In fact, the '111 patent discloses nothing about the feature of subdividing memory for ANY purpose.

Applicants note that the frame buffer 134 of the '111 patent comprises a number of memory devices, such as VRAMs 210, 220, 230, which are required because of the large amount of pixel data to be stored to achieve a desired resolution for the display screen. As stated in the '111 patent:

> "[I]t is desirable to provide a frame buffer for storing pixel data for a 1024x768 display screen resolution. Illustratively, 1 Mbyte (1,048,576 byte) VRAMs are used and each pixel is represented by 32 bit data. Using a linear addressing scheme, only three 1 Mbyte VRAMs 210, 220 and 230 are necessary to store the pixel data." Col 8, ll. 46 – 53.

In other words, the memory devices comprise the frame buffer. Applicants note that the '111 patent does not disclose subdividing the memory region into a plurality of sub-regions. The system of the '111 patent does not include any functionality or structure that subdivides the memory into a plurality of sub-regions for the purpose of clearing data stored in the memory.

Furthermore, because the '111 patent fails to disclose, teach, or suggest subdividing the memory region to be cleared into a plurality of sub-regions, Applicants respectfully submit that the '111 patent CANNOT disclose, teach, or suggest concurrently writing clear data to the sub-regions. In this regard, Applicants respectfully submit that the graphics system of the '111 patent does NOT include any component which "subdivides a region of the frame buffer into a plurality of sub-regions" and "concurrently writes clear data to each of the plurality of sub-regions." The memory devices of the '111 patent are merely individual memory devices that store pixel data for the frame buffer. The '111 patent does not disclose anything about subdividing a region of the frame buffer 134 to be cleared. Furthermore, Applicants note that the '111 patent does not disclose anything about concurrently writing clear data to each of the plurality of sub-regions. In fact, the Office Action admits that the '111 patent "did not explicitly disclosed (*sic*) that the controller is designed to write clear data concurrently to each of said plurality of sub-regions."

Unlike the '111 patent, claims 15, 20, 21 and 24 recite a method, computer-readable medium, system, and graphics system (respectively), each of which recite subdividing a memory region to be cleared into a plurality of sub-regions. The memory region is not merely one of the memory devices that comprise the memory (as disclosed in the '111 patent). Rather, the memory region being subdivided corresponds to a region of the memory to be cleared. As stated in the specification of the present application, the amount of time required to clear a portion of the display screen may be reduced by subdividing the region to be cleared into a plurality of sub-regions and concurrently writing clear data to each sub-region.

Applicants respectfully assert that the '297 patent also fails to disclose the features of subdividing a memory region to be cleared into a plurality of sub-regions and concurrently writing clear data to each of the sub-regions. The Office Action alleges that the '297 patent discloses "a graphics update controller being able to write simultaneously clear data into a plurality of VRAM chips in the frame buffer." The Office Action further alleges that it would have been obvious to a person of ordinary skill in the art at the time the invention was made "to have utilized the controller taught by [the '297 patent] into the system of [the '111 patent] because doing so would provide an efficient method for clearing of a region of the screen by writing a plurality of bits into a plurality of pixels in the frame buffer."

Applicants respectfully submit that the '297 patent merely describes a frame buffer such as that described above with respect to the '111 patent. Specifically, Applicants note that the '297 patent merely discloses a frame buffer 3, 15 comprising a plurality of memory devices, such as VRAM chips. Similar to the '111 patent, the plurality of memory devices in the '297 patent (*i.e.*, the individual VRAMs that define the frame buffer) are merely individual memory devices that store pixel data for the frame buffer. The '297 patent does not disclose anything about subdividing a region of the memory to be cleared into a plurality

of sub-regions. Furthermore, because the '297 patent fails to disclose, teach, or suggest subdividing the memory region to be cleared into a plurality of sub-regions, Applicants respectfully submit that the '297 patent CANNOT disclose, teach, or suggest concurrently writing clear data to the sub-regions. Rather, the '297 patent merely appears to suggest simultaneously clearing each of VRAMs that define the frame buffer.

In fact, Applicants note that both the '297 patent and the '111 patent would benefit from Applicants' invention. The method and apparatus of the '297 patent would be able to more quickly clear a region of the z-buffer if the video display system included the features of subdividing a region of the z-buffer to be cleared into a plurality of sub-regions and concurrently writing clear data to each of the sub-regions. Furthermore, the screen refresh controller of the '111 patent would be enhanced by adding the features of subdividing a region of the frame buffer into a plurality of sub-regions and concurrently writing clear data to each of the sub-regions because less time would be required to clear the region.

With regard to the other cited references, Applicants note that the Office Action does not allege that these claimed features are disclosed, taught, or suggested by the '382 patent or the '306 patent. In fact, Applicants reviewed the entirety of these references and respectfully submit that these features are not disclosed, taught, or suggested by any of the references. Accordingly, Applicants respectfully submit that independent claims 15, 20, 21 and 24 are patentable over the cited art for at least the reason that the references fail, either individually or in combination, to disclose, teach, or suggest the claim features/limitations/elements discussed above. Dependent claims 16 – 19 (which depend from independent claim 15), dependent claims 22 and 23 (which depend from independent claim 21), and dependent claims 25 – 28 (which depend from independent claim 24) are also patentable over the cited art of record for at least the reason that the claims include all of the

features/limitations/elements of the corresponding base claim. Accordingly, Applicants respectfully request that the rejection of claims 15 – 23 be withdrawn and claims 15 – 23 (and new claims 24 – 28) be allowed.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been rendered moot, and that pending claims 15 – 28 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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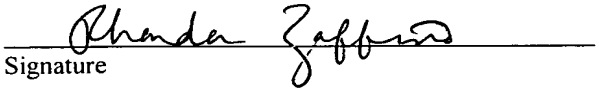

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